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PHOTOLITHOGRAPHIC METHODS FOR MAKING LIQUID-CRYSTAL-ON-SILICON DISPLAYS WITH ALIGNMENT POSTS AND OPTICAL INTERFERENCE LAYERS

This is related to Patent Application Serial No._____ by Su Yong Jie, Ravi Sankav and Han Zhi Ciang filed as _____ (CS 98-077) and to Serial No. _____ by Sudipto R. Roy filed as _____ (CS 98-078), all of Chartered Semiconductor Manufacturing LTD of Singapore Technologies.

BACKGROUND OF THE INVENTION

(1) Field of the Invention

This invention relates to new methods of photolithographic fabrication of alignment posts and optical interference layers directly on liquid-crystal-on-silicon displays.

(2) Description of the Prior Art

The picture quality of liquid crystal displays from the simple seven segments to millions of pixels is determined by the structure used to control the variation of thickness and position leads after wafer processing. There are known processes for creating insulated alignment posts based on preformed glass micro-spheres and rods; relatively low series resistance posts can be obtained by means of selective deposition of polysilicon and metallic silicide.

(The making of metallic vias and contacts is a comparatively well known processing art.)

US Patent 5,498,925 to Bell et al describes the formation of posts in flat panel displays using processes based on a heat-treated slurry or paste upon a glass plate. US Patent 5,597,736 teaches the function of a light-blocking layer deposited upon a semiconductor substrate material that can emit light. US Patent 5,744,824 and US 5,748,828 show various LCD structures and external optics.

Until now, it has been difficult to construct alignment posts using photolithography and also add optical interference layers simultaneously onto a semiconductor substrate material used to control the gray-level of each pixel.

BRIEF SUMMARY OF THE INVENTION

A principal object of the present invention is to describe various new methods for building a flat-panel liquid-crystal display upon an integrated circuit (IC) die with inter-related alignment between the posts supporting the overlaying glass cover plate and optical interference layers employed to improve image quality.

Another object of this invention is to describe effective and very manufacturable methods of photolithographic formation of insulating alignment posts (also called studs or pillars). These methods can be used in processing many different device types, and are described in this application for liquid crystal display devices as a way of illustrating their embodiment at a pixel density beyond that achievable with preformed micro-glass spheres and rods.

A further object of the present invention is to describe methods of deposition for both the posts and the optical interference layers that are independent of each other and retain their desired feature during deposition of subsequent features. The various methods are classified into five method categories: 1) silicon oxide wet etching; 2) amorphous silicon plasma etching; and 3) nitride plug filling; 4) insulating material lift-off; 5) photosensitive polyimides.

Five new methods for the formation of an improved liquid-crystal-on-silicon display are described, in which the device structure is enhanced by the photolithographic building of alignment posts among the mirror pixels of the micro-display. At the same time these five methods accommodate the fabrication of an optical interference

multilayer that improves the image quality of the reflected light. These five methods are:

Silicon Dioxide Posts by Wet Etching - wherein said alignment posts are formed by the process of silicon dioxide wet etching upon the said silicon substrate.

Amorphous Silicon Posts by Plasma Etching - wherein said alignment posts are formed by the process of amorphous silicon plasma etching upon the said silicon substrate.

Silicon Nitride Posts by Plug Filling.- wherein said alignment posts are formed by the process of silicon nitride plug filling upon the silicon substrate.

Insulation Material Posts by Lift-Off - wherein said alignment posts are formed by the process of insulation material lift-off upon the said optical interference layer OIL.

Polyimide Posts by Photosensitive Etching - wherein said alignment posts are formed by the process of polyimide photosensitive etching upon the OIL.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings forming a material part of this description, there is shown:

Figs. 1 through 3 schematically illustrate in cross-sectional representation a preferred embodiment of the device structure of the present invention. The base silicon substrate with the formed metallic pixels on the display device is shown in Fig. 4.

The process flow for making the alignment posts and the optical interference layers by the five process categories is shown in Figs. 5 to 19.

Fig. 5 shows a detailed cross-sectional diagram of the device ready to be covered with the optical interference layers.

Fig. 6 shows the optical interface layers deposition.

Fig. 7 shows the thick silicon oxide layer deposit on top of the OIL.

Fig. 8 shows the photomask after etch off of the excess silicon oxide with wet etch.

Fig. 9 shows the thick amorphous silicon deposition on top of the OIL.

Fig. 10 shows the result of post photomasking and plasma amorphous silicon etching.

Fig. 11 shows the thick oxide layer deposition of top of the OIL used in forming the plugs of silicon nitride.

Fig. 12 shows the result of post photomasking, plasma oxide etching and plasma enhanced nitride chemical vapor deposition.

Fig. 13 shows the result of silicon nitride etch-back with plasma and oxide removal with wet etching.

Fig. 14 shows the result of the deposition consequence of a thick photoresist, SiO by thermal evaporation, and a thin resist layer prior to the deposition of the insulation material posts.

Fig. 15 shows the result of the photomasking, plasma etching the SiO layer and another plasma etch of the bottom resist prior to the deposition of the insulation material.

Fig. 16 shows the cross-section after the thermal or electron beam evaporation of insulation material.

Fig. 17 shows the cross-section after the photoresist lift-off in an ultrasonic bath of resist remover.

Fig. 18 shows the cross-section after the photosensitive polyimide is deposited.

Fig. 19 shows the cross-section after the post photomasking and development of the photosensitive polyimide.

Fig. 20 schematically illustrates in cross-sectional representation one type of final embodiment of this invention for this liquid-crystal-on-silicon display device.

Fig.21a and Fig. 21b illustrate (by means of a top view) how the display device can be constructed with the alignment posts between the pixels.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now more particularly to Fig. 1, here is shown a portion of a partially completed integrated circuit liquid-crystal display. The glass cover plate 10 provides the transparent enclosure for the external incident light to be reflected back to an observer. The strength of reflected light is dependent on the light polarization, absorption and

light scattering properties of each liquid-crystal display pixel, which is controlled by the electrical field established within the liquid crystal material 11. The IC die 12, separated from the glass plate by the alignment posts 14 generates these E-fields. The resultant space between the glass plate and the silicon wafer is filled with the chosen liquid crystal material. Light, either provided or ambient, enters the open face of the liquid-crystal-on silicon and is reflected from the underlying pixels to form a viewable pattern of polarized light, i.e. the image is viewed directly or projected through an optical polarized system.

Fig.2 illustrates the bonding pads 20 on the IC die to which the external wires 22 are attached. The silicon wafer contains the embedded control circuits that activate the pixel patterns in the viewable area 24. The optical properties of the liquid crystal (e.g. the rotation of plane-polarized light or the dispersion of light) are influenced by the electric fields above the IC surface. A small change in voltage makes a large change in the optical transmission. Because this invention teaches the photolithographic making of patterns of alignment posts, the ratio of pixels 30 to posts 14 is often fabricated in the range 1:1 to 1:10000. As shown in Fig. 3, the photolithographic method permits these alignment posts to be constructed in the space between adjacent pixels.

The process steps for making the alignment posts and optical interference layers by means of the various photolithographic categories is shown in Figures 4 to 20.

Starting with Fig. 4, the conductive metallic (or poly) layer 30 is formed over the silicon oxide 40, which is formed on top of the second metal layer 20 on the IC. Prior to formation of the silicon oxide 40, the metal 20 as bond pad is deposited on silicon dioxide layer 41. A silicon semiconductor substrate 09 is coated with an silicon dioxide insulating layer 15 and has active devices therein and an metal layer (metal 1) 16 upon which silicon dioxide layer 41 is formed. Then a photoresist layer is formed over the metal 30 to construct the pixels. The photoresist is exposed and a portion removed to provide that each pixel retains a metallic layer, which shall act as a mirror reflector for the light incident upon said pixel.

After the resist is stripped, as shown in Fig. 5, the device is ready to be covered with the optical interference layers 60. Optical interference layers are used to improve light reflections. Careful attention is required in constructing these optical interference layers so as not to disturb any underlying devices and/or posts. Fig. 6 shows the resultant structure, which is ready for the fabrication of alignment posts.

The optical interference layer coating (OIL) is composed of oxides and nitrides, coated into multiple layers of insulating material with properties of varying optical indices of refraction. The alignment posts are constructed after the OIL is made by one of the five process methods described herein:

Method 1 - Silicon Dioxide Posts by Wet Etching

A silicon oxide layer 70, about 1 micron thick, is deposited on top of the OIL 60, as shown in Fig. 7. The photomask 80, about 4 microns across, is formed at the location of each alignment post, and a wet etch, such as hydrogen fluoride or buffered HF, is applied to remove the excess silicon oxide. The resultant alignment posts 71 are shown in Fig. 8 (in this illustration on the peripheral). After removing the alignment post photoresist, a photomask is deposited to make the metal bonding pad 20, and the said pad is etched into the OIL 60 plus silicon oxide 40, followed by the removal of this photomask and formation of the bond pads 20.

Method 2 - Amorphous Silicon Posts by Plasma Etching

An amorphous silicon layer 90, about 1 micron thick, is deposited on top of the OIL 60, as shown in Fig. 9. The

photomask 100, about 2 microns across, is formed at the location of each alignment post, and a plasma silicon etch, such as CF4/O2 or SF6, is applied to remove the excess amorphous silicon. This plasma etch has a high selectivity in the presence of silicon nitride, and will not damage the silicon nitride top layer in the OIL 60. The resultant alignment posts 101 are shown in Fig. 10 (in this illustration between the pixels). This process method is completed as described in Method 1, by removing the photoresist 80 and formation of the bond pads 20.

Method 3 - Silicon Nitride Posts by Plug Filling

A silicon oxide layer 110, about 1 micron thick, is deposited on top of the OIL 60, as shown in Fig. 11. The photomask is formed over the oxide, except the location of each alignment post, and a plasma oxide etching is used to remove the silicon oxide not covered by the photomask, creating cavities 120, including some or all of the OIL at the base of the post cavity. Subsequently the post cavities 120 are filled with silicon nitride 121 deposited by plasma enhanced chemical vapor deposition (PECVD). [The plasma enhancement provides low temperature deposition (about 200 degrees centigrade) during the deposition over that obtained without the existence of the plasma. Without the plasma, the nitride deposition is in the range of 700 degrees centigrade.]

Subsequently a silicon nitride etch-back (also using a plasma etch) removes all the PECVD nitride except the cavity plugs 122. The plug filling of silicon nitride is not totally etched away by the plasma because the plasma etching is stopped after the nitride at the surface is removed. The remaining oxide 110 is removed with a wet etch, such as HF or buffered HF, as shown in Fig. 13. The wet etch does not remove the silicon nitride plugs because the selectivity between SiO2 and the nitride is infinite for HF etching, nor the OIL top layer because it is also a nitride. This process method is completed by formation of the exposed bond pads 20, as shown previously via a top sectional view in Fig. 2, and again later in a cross-sectional view in Fig. 20.

Method 4 - Insulation Material Posts by Lift-off

A photo resist or PMMA acylic layer 140, about two microns thick, is formed on top of the OIL, and a silicon monoxide layer 141 is placed over the photoresist 140 by thermal evaporation. These steps are followed by formation of another photoresist layer 142, about 1 micron thick, upon the silicon monoxide 141, as shown in Fig. 14. After photomasking the photoresist 142 is developed to expose the location of the plugs 150, the SiO layer 141 is etched with a CF4 plasma and the bottom photoresist 140 is etched with an oxygen plasma, as shown in Fig 15. The cavities 150 in

the bottom thicker photoresist are then filled with insulation material 152, (calcium fluoride, silicon monoxide, yttrium oxide, aluminum oxide) by thermal or electron beam evaporation; E-beam evaporation is shown in fig. 16. The electron beam 160 is deviated by a magnetic field to strike on the material source, which is then evaporated and deposited onto the wafer. Control of the amount of the material evaporated is normally done by a crystal film thickness monitor. The bottom photoresist 140, silicon monoxide 141, and everything on top of SiO is removed by an acetone (or similar) ultrasonic bath, as shown in Fig. 17. The resist removal processing step does not affect the insulation material posts because these materials do not dissolve in acetone and stick well to the substrate. The posts made of insulation material are left among the pixels as shown, or around the peripheral as described in a prior method of this application. The process method is completed by formation of the bond pads 20.

Method 5 - Polyimide Posts by Photosensitive Etching

A photosensitive polyimide layer 180, about 1 micron thick, is formed on top of the OIL 60, as shown in Fig. 18. The photosensitive polyimide is deposited by spinning. This layer 180 is exposed to an UV light pattern so as to develop the polyimide to be used as the alignment post material. The unexposed photosensitive polyimide is then removed by

development, as shown in Fig. 19, leaving the polyimide posts 191. This process method is completed by the formation of the bond pads 20.

To complete the IC packaging, the IC is mounted onto a lead film and wires (22) are bonded from the legs of the lead film to the metal pad 20, as shown in Fig. 20.

The top-view of one possible display device layout, shown in Fig. 21a and Fig. 21b, illustrates the location of the alignment posts, for example 191. While this drawing shows the posts 191 to be located among the metallic pixels 30, an alternative design would have some or all the alignment posts intermixed with the bonding pads 20 on the peripheral.

For all five methods of photolithographic formation of alignment posts on LCD-on-silicon display devices, the existence of numerous alignment posts permits the usage of an ultra-thin glass plate or cover over the liquid crystal. Both the worbpage of the wafer and the glass plate do not affect the thickness of the LCD material. This implementation results in lightweight displays for portable applications. Glass covers supported by alignment posts are typically 0.5 millimeters in thickness, and can range from 0.1 mm to 2 mm.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

WHAT IS CLAIMED IS: